SleepWalker: A 25-MHz 0.4-V Sub-mm² 7-μW/MHz Microcontroller in 65-nm LP/GP CMOS for Low-Carbon Wireless Sensor Nodes

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Abstract—Integrated circuits for wireless sensor nodes (WSNs) targeting the Internet-of-Things (IoT) paradigm require ultralow-power consumption for energy-harvesting operation and low die area for low-cost nodes. As the IoT calls for the deployment of trillions of WSNs, minimizing the carbon footprint for WSN chip manufacturing further emerges as a third target in a design-for-the-environment (DfE) perspective. The SleepWalker microcontroller is a 65-nm ultralow-voltage SoC based on the MSP430 architecture capable of achieving improved speed performances at 25 MHz for only 7 μW/MHz at 0.4 V. Its sub-mm² die area with low external component requirement ensures a low carbon footprint for chip manufacturing. SleepWalker incorporates an on-chip adaptive voltage scaling (AVS) system with DC/DC converter, clock generator, memories, sensor and communication interfaces, making it suited for WSN applications. An LP/GP process mix is fully exploited for minimizing the energy per cycle, with power gating to keep stand-by power at 1.7 μW. By incorporating a glitch-masking instruction cache, system power can be reduced by up to 52%. The AVS system ensures proper 25-MHz operation over process and temperature variations from −40°C to +85°C, with a peak efficiency of the DC/DC converter above 80%. Finally, a multi-Voltage clock tree reduces variability-induced clock skew by 3× to ensure robust timing closure down to 0.3 V.

Index Terms—CMOS digital integrated circuits, design for the environment (DfE), near-threshold/subthreshold logic, system-on-chip (SoC), ultralow power, ultralow voltage, variability mitigation.

I. INTRODUCTION

The vision of the Internet-of-Things (IoT) as the core of the Web3.0 targets the development of ambient intelligence with wireless sensor nodes (WSNs) attached to every object [1]. Such WSNs will feature sensing and computing capabilities with memories, energy management and wireless communication to allow interaction with the cloud. The IoT will enable exciting new applications in fields such as energy savings, habitat, transportation, healthcare, entertainment and security. Design targets for the systems-on-chip (SoCs) in this context are ultralow power consumption for energy-autonomous operation (energy harvesting or decade-long battery autonomy) and low die area for cost efficiency.

To support these applications, trillions of connected WSNs need to be deployed [2]. With such a huge number of WSNs, the development of the IoT could be detrimental for the quality of our environment. The energy consumed by the ultralow-power WSNs during the use phase of their life cycle is negligible from an environmental stand point [3]. However, the energy-intensive chip manufacturing raises concerns in terms of resource depletion (energy, water and materials), global warming potential, human health hazards and ecotoxicity [4]. As an example, we estimate that the production of 1000 cubic-millimeter WSNs such as [5] represents a carbon footprint around 300 kg CO₂e.¹ This accounts for 1.5% of the annual carbon footprint of an average U.S. citizen [6]. As the environmental impact of chip manufacturing scales directly with the die area, compact on-chip design is also paramount in a design-for-the-environment (DfE) perspective to leverage a sustainable development of the IoT.

In this paper, we present the design of the Sleepwalker microcontroller for low-carbon WSNs [7] featuring sub-mm² die area and a record active power of only 7 μW/MHz at full SoC level. We designed it for 25-MHz operation, which is a relatively high speed for ultralow-power SoCs [5], [8]–[15], to specifically address the development of future IoT applications demanding more computing power. Instead of the conventional 1–1.5-V design of microcontrollers in 0.18-/0.13-μm CMOS [13], [14], we leverage an ultralow-voltage (ULV) design at 0.4 V in 65-nm CMOS for concurrent minimization of active power [16] and die area. ULV operation in 65-nm CMOS leads to design challenges in terms of robustness (noise margins, timing closure), sensitivity to process, voltage and temperature (PVT) variations and stand-by leakage power [17] that we

¹Data in the conventional metric for global warming potential (GWP) based on the model from [4] as updated in [3] for 300-mm bare silicon wafer production and CMOS process, while assuming a total silicon area of 15 mm² (stacked dies) per WSN and a Taiwan-based production site.
Fig. 1. SleepWalker SoC overview. (a) System architecture and partitions. (b) \( V_{dd}/V_{t} \) selection for minimization of active energy under the 25-MHz timing constraint (SPICE simulations of the 80FO4 critical path @TT 25 °C). Versatility of the LP/GP process allows operating each partition close to the MEP at 25 MHz.

overcome compromising neither density, functionality, nor speed performance thanks to:

- a dual-\( V_{dd} \)/multi-\( V_{t} \) system partitioning in an LP/GP process mix;
- a glitch-masking ULV instruction cache with no cache miss latency;
- an all-digital on-chip adaptive voltage scaling (AVS) system with integrated switched-capacitor DC/DC converter;
- a multi-\( V_{t} \) ULV clock tree for reliable timing closure with low-power SoC features;
- a strict high-density design approach at system and block levels.

This paper is organized as follows. In Section II, we present the system design including partitioning and the proposed instruction cache. The AVS system is detailed in Section III with the integrated DC/DC converter. Section IV unveils the physical implementation to ensure robust timing closure and maximum energy efficiency at ULV. Finally, the test chip and measurement results are presented in Section V.

II. SYSTEM DESIGN

A. SoC Overview

Fig. 1(a) gives an overview of the SleepWalker microcontroller SoC. The 16-b CPU is organized around an open-source core [18], compatible with the MSP430 instruction set and cycle accurate with its original architecture, that we modified at the RTL level for improved energy efficiency via multiple clock domains and data gating on buses. The open-source core features several peripherals including an interrupt controller (not represented), special function registers (SFR), a 16-b hardware multiplier (MULT), GPIO ports, a watchdog (WDT) timer, and a debug UART. We further added key peripherals: two master SPI interfaces, a 16-b timer, clock management and clock synchronization units, sleep, and AVS controllers. A 16-b time-to-digital (TDC) converter is integrated for interfacing frequency-output sensors such as [19] with an eight-entry FIFO to minimize the number of wake-up cycles in acquisition. RAM memories of 16 and 2 kB are integrated for program (PMEM) and data (DMEM) memories, respectively. The DMEM is substantially smaller than the PMEM because we target control applications. A synthesized bootloader (BL) ROM is implemented in the memory management unit with an instruction cache (IS) for low power, as discussed in the next sections.

The microcontroller is designed for 25-MHz operation to provide relatively high real-time computation power. As the peripherals require much lower data rates, we also included configurable clock division units (prescalers) for the timer, the TDC, and both SPI modules, to save switching power.

B. \( V_{dd} \) and \( V_{t} \) System Partitioning

Ultralow-voltage (ULV) operation of digital circuits is capable of minimizing the energy per cycle \( E_{cycle} \) down to the minimum energy point (MEP) [20], which results from a tradeoff between switching energy \( E_{sw} \) proportional to \( V_{dd}^{2} \) and leakage energy \( E_{leak} \) from leakage power integrated over the cycle time \( T_{cycle} \). For a given circuit topology and CMOS process, the MEP is defined by its \( E_{cycle} \) level associated with a single clock frequency \( f_{MEP} \) and a single supply voltage \( V_{MEP} \) [17]. This MEP is highly sensitive not only to PVT variations but also to circuit parameters such as the switching activity factor \( \alpha_{F} \) that impacts the \( E_{sw}/E_{leak} \) ratio [20].

A key target for ULV design is to align the frequency of the MEP \( f_{MEP} \) to the target frequency of the application \( f_{target} \) [21], which is 25 MHz for SleepWalker. Indeed, if \( f_{target} > f_{MEP} \), the circuit violates the setup timing constraint at \( V_{MEP} \), and if \( f_{target} < f_{MEP} \) energy is wasted because
leakage power is integrated over a prohibitively long cycle time. In 65-/45-nm CMOS processes featuring many-Vt options, this can be achieved through the proper selection of the MOSFET Vt to implement the ULV digital circuit [21]. For the SleepWalker microcontroller, we selected a 65-nm CMOS technology that offers a versatile menu of transistors thanks to a low-power/general-purpose (LP/GP) process mix [22]. The LP process features transistors with a thick core oxide and a printed gate length Lg equal to the drawn Lg (minimum 60 nm), which result in a low gate leakage and a high Vt, for a given channel doping level. The GP process, also called ‘generic’ by some foundries, features a thin core oxide with a scaled printed Lg (minimum 45 nm corresponding to a drawn Lg of 60 nm), which result in higher gate leakages and lower Vt levels. At a given ULV supply, the GP flavor brings a huge delay reduction as the MOSFETs move from the sub- to near-threshold regime [23]. Process selection thus allows shifting fMEEP from the 50–500 kHz range for the LP process, to the 10–50 MHz range for the GP process [23]. In this 65 nm LP/GP CMOS, 3 doping levels are available for core MOSFETs, which gives a total of 6 possible Vt values available on the same die at low mask count (in Vt decreasing order): HVT/SVT/LVT in the LP process and HVT/SVT/LVT in the GP process.

System simulations of the microcontroller in typical WSN scenarios show that in active mode, the blocks from Fig. 1(a) experience very different activity factors (αF): 10–50% for the CPU, 0.2–5% for memories (depending on the hit rate of the instruction cache) and very low αF < 0.1% for always-on peripherals (AOPs) such as the timer and the TDC. SPICE simulations in Fig. 1(b) show how the MEP voltage VMEP varies with αF: the large Esw contribution to EMEP at high αF calls for low Vdd (0.4–0.45 V for the CPU), whereas the high leakage contribution at low αF calls for a short cycle time and thereby a high Vdd (0.5–0.7 V for memories, and 1–1.1 V for AOPs). To support the 25-MHz timing constraint at VMEP, the Vt needs to be adjusted, as shown in Fig. 1(b). The CPU is optimally implemented with GP SVT MOSFETs in a 0.4 V ULV power domain (near-Vt regime), whose supply voltage is generated on-chip by the AVS system described in Section III. The drawback of the GP process is its high leakage current which is only slightly mitigated by the ULV operation through reduced drain-induced barrier lowering (DIBL) effect. In order to avoid ruining the standby power, the ULV power domain thus needs to be power gated.

Without an instruction cache, the program memory PMEM would be optimally implemented with GP HVT MOSFETs at 0.5 V. However, this raises two issues, given here.

- Low density: relatively large bitcells with 8–12 transistors [24]–[27] must be used to alleviate vanishing noise margins in subthreshold SRAM memories.
- High standby power: the need for data retention prevents the use of power gating to mitigate the relatively high leakage level of GP HVT MOSFETs.

Therefore, subthreshold SRAM is not the best option for the low die area target and we selected the highest available Vt (LP HVT) with the dense 6 T SRAM macros from the foundry (0.5 μm2 bitcell) for both program (PMEM) and data (DMEM) memories. They are operated at the 1–1.2-V external Vdd, which is also used for the I/Os and AOPs. To limit the Esw overhead of the 1-V PMEM, we implement an instruction cache within the ULV power domain that is presented in Section II-C. In Sleep-Walker, the DMEM does not require a cache memory because its Esw is lower thanks to its smaller size of 2 kB (shorter bitlines) and less frequent access.

C. Glitch Masking Instruction Cache

The instruction cache (IS) from Fig. 2(a) is implemented in the ULV power domain with a simple direct-mapped organization without write-back policy. It is synthesized using standard-cell flip-flops to limit noise margin issues at ULV. As shown in [12], when a ULV cache is associated with a higher voltage SRAM memory, it is possible to fetch the instruction in case of a cache miss within the same cycle thanks to fast access and setup times of the main memory at a higher Vdd, i.e., the 1-V PMEM in our case. This requires direct connection of the address bus to the PMEM, which generates glitches on the level shifters with a proportionally high Esw overhead. We therefore added the glitch masking circuitry depicted in Fig. 2(a), which allocates the first half of the clock cycle to the generation of the hit signal before conditionally opening the connection to level shifters in case of a cache miss, when the address is stable. This allows saving up to 30% of the cache switching power (at 100% hit rate).

For full glitch masking, the critical path (CP) delay for generation of the hit signal should be lower than half Tcycle. As shown in Fig. 2(b), the cache size strongly impacts the hit delay and the area of the ULV power domain. We selected 32 entries (16-b words) as a low-overhead choice to keep die area minimal. The power overhead of adding the cache in the ULV domain is 33% while it allows saving 21%–52% of total system power with typical hit rates of 50%–100%.
III. ALL-DIGITAL ON-CHIP AVS SYSTEM

The speed of ULV digital circuits is highly sensitive to PVT variations. Therefore, they require a large $T_{\text{cycle}}$ guardband to ensure safe setup timing closure [17]. For the SleepWalker CPU at 0.4 V, the $T_{\text{cycle}}$ increase due to worst case corner for speed is 250%. This worst case corner appears with a SS process at $-40 \, ^\circ\text{C}$ because low temperature has the most detrimental impact on speed at ULV [28]. To alleviate the PVT impact on gate delay, we designed an all-digital on-chip adaptive voltage scaling (AVS) system based on the theoretical principles from [29]. Its purposes are as follows.

- generation of the regulated 25 MHz clock;
- generation of the regulated internal $V_{\text{id}}$ for the ULV domain from the unregulated (1–1.2 V) external $V_{\text{id}}$;
- dynamic adaptation of the internal $V_{\text{id}}$ to compensate delay variations from process and temperature changes.

The internal $V_{\text{id}}$ needs to be adapted from 0.48 V to compensate the SS process at $-40 \, ^\circ\text{C}$ to 0.32 V for power savings in the FF corner at $+85 \, ^\circ\text{C}$.

The AVS regulation loop, depicted in Fig. 3, uses a critical-path replica ring oscillator (CPR RO) to both generate the 25-MHz clock and sense the critical path delay, while a crystal clock (off-chip in the SleepWalker prototype) serves as a time reference. The information about the CPR RO frequency is sent to the AVS controller which decides to either increase or decrease the internal $V_{\text{id}}$. This internal $V_{\text{id}}$ is generated by a switched-capacitor DC/DC converter controlled via a frequency modulation scheme by a variable-length RO.

An AVS system based on a comparable principle was recently proposed in [9] but our AVS system is fully designed for low-carbon WSNs in 65-nm CMOS. This necessitates: 1) an on-chip implementation with a switched-capacitor DC/DC converter to avoid both the cost and carbon footprint of external inductors and 2) an all-digital loop with frequency modulation and a simple low-power regulation scheme for low die area.

A. AVS Controller

The AVS controller monitors the frequency generated by the CPR. The delay of the critical paths (CPs) depends on both gate and $RC$ interconnect delays [31], [32]. However, $RC$ delays have small contributions to the critical paths of the SleepWalker CPU because: 1) the CPU area is small, which means short wires between gates in the CPs and 2) at ULV RC delays are proportionally smaller than gate delays [30]. Furthermore, the standard cells from the ULV library we generated all feature the same gate length and have transistor stacks limited to 3, as explained in Section IV-C. Therefore, a CPR RO made of NAND2 and NOR2 gates from this library realistically captures global PVT variations of the actual CP delays, while being an efficient solution in terms of area and design cost. A small guardband is included though to ensure safe operation versus within-die (WID) variations and behavior differences between the CPR RO and these actual critical paths. A 10-b counter counts the number of rising edges of the CPR RO during the low phase of the crystal clock. The result is compared to a target count corresponding to the 25 MHz $f_{\text{target}}$. If the CPR RO frequency is lower (resp. higher) than $f_{\text{target}} \pm 0.5$ MHz, the AVS controller requests an increase (resp. decrease) of the internal $V_{\text{id}}$ to correct the CPR RO frequency.

A simple $+/1$ regulation is chosen to keep both the power consumption and the area of the AVS loop low, at the cost of a slow loop response. This is acceptable because the AVS feedback loop has to track process and temperature variations, which are slow. Moreover, the CPR RO is supplied by the low internal $V_{\text{id}}$, ensuring that no timing violation from fast transient voltage or workload fluctuations can occur in the ULV power domain [29].

The AVS controller with the Dec and Sync registers of the variable-length RO (Section III-C) are synthesized from RTL with automatic clock gating in the 1 V power domain with the always-on peripherals (AOPs). The power consumption from physical synthesis is 1.3 $\mu$W in typical conditions.
B. DC/DC Converter

The DC/DC converter performs the DC/DC voltage down conversion from the external 1–1.2-V \( V_{dd} \) to the 0.32–0.48-V internal \( V_{dd} \) used by the ULV power domain. It is built with two interleaved switched-capacitor networks (SCNs) to limit the voltage ripple on the internal \( V_{dd} \). The SCNs use a divide-by-two topology using five power switches. The body voltage of the switches connected to the converter output (internal \( V_{dd} \)) and of the switch between transfer capacitors \( C_{Ta} \) and \( C_{Tb} \) is biased at the internal \( V_{dd} \). This alleviates the negative body bias normally seen by these devices when they are ON, leading to a 38% switch size reduction and thus lowering the associated gate drive losses. In standby mode, the DC/DC clock is stopped and the switches act as power-gating sleep transistors, which is required to limit the leakage power of the ULV domain implemented with low-\( V_T \) MOSFETs (GP SVT), as explained in Section II-B. Reducing the switch sizes thus leads to a direct reduction of this leakage in standby mode [33]. For leakage power reasons, LP MOSFETs are used to implement the switches.

The SCNs use MIM capacitors as transfer capacitors \( C_{Ta} \) and \( C_{Tb} \) for compact on-chip implementation. Furthermore, \( C_{Tb} \) is physically implemented at the layout level above the 1-V power domain of the AOPs. The switching noise from \( C_{Tb} \) does not harm the operation of AOPs because: 1) the bottom plate of \( C_{Tb} \) is always connected to the ground, acting therefore as a shield and 2) because AOPs have low noise sensitivity thanks to both their 1–1.2-V \( V_{dd} \) and their loose timing constraints, as most logic paths operate on the crystal clock. This stacking of MIM capacitors allows recycling 44% of the converter area. The converter area is only 0.07 mm\(^2\) thanks to this MIM stacking scheme, i.e., 40% smaller than the converter from [15], designed to supply a sub-MHz microcontroller at 0.5 V. Further reduction in the converter area could be achieved through the study of other SCN topologies as shown in [34]. The sizing of \( C_{out} \) results from a tradeoff between the low ripple target (20 mV) on the internal \( V_{dd} \) and a short wake-up time (<1 crystal clock cycle = 10 \( \mu s \)).

C. Variable-Length Ring Oscillator

As long as the charge transfer is not limited by the conductance of the power switches (i.e. the converter is in the slow-switching-limit regime), the power delivered by the converter to the ULV power domain is given by [35]

\[
P_{out} = f_{sw} \times C_T \times V_{out} \times (V_{in} - V_{out})
\]

where \( f_{sw} \) is the converter switching frequency, i.e., the frequency of DC/DC clock from Fig. 3, \( C_T \) (400 pF) is the sum of \( C_{Ta} \) and \( C_{Tb} \) of both SCNs, \( V_{out} \) is the internal \( V_{dd} \) and \( V_{in} \) is the output voltage of the converter when no load is applied, i.e., half the 1–1.2-V external voltage. According to (1), for a given \( P_{out} \), the internal \( V_{dd} \) can be controlled by modulating \( f_{sw} \). A variable-length RO is thus implemented to generate the DC/DC clock. When the AVS controller requests a higher (resp. lower) internal \( V_{dd} \), the RO length is reduced (resp. increased), thereby increasing (resp. reducing) \( f_{sw} \).

To avoid interrupting the DC/DC converter, the RO length is adapted dynamically. On the crystal-clock falling edge, the controller sends the request for increasing or decreasing the internal \( V_{dd} \). In order to avoid parasitic oscillation in the RO, control signals from the synchronization register are sent when the oscillating edge propagates in the fixed-length part of the oscillator, as shown in Fig. 3. The incremental parts of the RO are thus reconfigured by the time the oscillating signal reaches them. The control signals from the AVS controller thus cross clock domains and a double register barrier is used to avoid metastability. The first register (Dec) decodes the signals from the controller into signals able to select the RO length. The second register (Sync) sends these signals to a multiplexer selecting the last stage of the RO and to NAND gates enabling incremental parts of the ring oscillator for low power.

From (1), the clock frequency range of the DC/DC converter needs to accommodate the wide range of the voltage drop \( (V_{in} - V_{out}) \) between 20 mV (conversion from 1 to 0.48 V \( V_{out} \) with a SS process at -40°C) and 280 mV (conversion from 1.2 V to 0.32 V \( V_{out} \) with a FF process at 85°C), as required by the high sensitivity of ULV circuits to PVT variations. Therefore, we chose a logarithmic scale for the length increment of each stage of the variable-length RO, responsible for generating this clock frequency. This achieves fixed relative frequency steps, rather than the fixed absolute frequency steps that would be achieved with a linear scale. With this logarithmic scale, we only need 31 different RO lengths to properly handle extreme conversion cases: low \( f_{sw} \) down to 1.65 MHz for 1.2- to 0.32-V conversion and high \( f_{sw} \) up to 17 MHz for 1.0- to 0.48-V conversion.

D. AVS Stability

The purpose of the AVS is to avoid the guardband due to PVT variations. The AVS feedback loop is much faster than a temperature change or a battery discharge, which thus do not threaten the system stability. However, a steep increase in the CPU workload may occur. In this case, additional charges needed by the CPU are taken from the 3.3-nF \( C_{out} \) for as long as the AVS feedback loop has not handled this power consumption increase. Because of the small amount of energy stored in \( C_{out} \), it leads to a lowering of the internal \( V_{dd} \), which threatens the CPU functionality if the internal \( V_{dd} \) drops under the functional limit. However, this drop is significantly limited by the reduction of the CPR frequency and thus the CPU power consumption when the internal \( V_{dd} \) decreases.

In order to prove the stability of the system, i.e., that the internal \( V_{dd} \) never drops below the functional limit, we simulated the following worst case: the CPU is first ideally clock gated so that the power of the ULV domain is only its leakage (33 \( \mu W \)) and a steep increase in the CPU workload occurs. The switching activity incurs a 50-\( \mu W \) step in the power consumption of the ULV domain. Fig. 4 shows that the internal \( V_{dd} \) first drops because of the small amount of energy stored in \( C_{out} \). The CPR frequency consequently drops simultaneously. These two factors reduce both the switching and leakage powers of the ULV domain. Furthermore, as the converter output voltage drops, the difference between \( V_{in} \) and internal \( V_{dd} \) increases, which in turn increases the power delivered by the converter as stated in (1). Therefore, the system stabilizes at an internal \( V_{dd} \) 60 mV.
below the target, which is still 40 mV above the functional limit [−0.3 V from measurement results in Fig. 7(b)]. The AVS regulation loop then detects the lower CPR frequency and starts to regulate the system to recover the target frequency within 100 μs.

IV. ULV PHYSICAL IMPLEMENTATION

The robustness of ULV circuits in nanometer CMOS technologies such as 65 and 45 nm is challenged by two main failure modes [17]: noise margin violations of logic gates which leads to stuck-at faults [36] and hold time violations [37]. Both failure modes are due to within-die (WID) variability (mismatch). Margining solutions such as MOSFET width upsize in the standard cells [36] are possible but incur area and energy overheads. Moreover, dual-V<sub>dd</sub> partitions and conventional low-power techniques such as automatic clock gating and multiple clock domains required for maximum energy efficiency further complicate the 25-MHz ULV timing closure at SoC level. For SleepWalker, we addressed these issues at the physical implementation level as detailed in this section.

A. Low-Variability ULV Clock Tree With Clock Gating and Clock Division

Whereas die-to-die (D2D) process variations are compensated by the AVS system, the relatively high WID V<sub>th</sub> variability in 65-nm CMOS still implies large random delay variations of logic gates at ULV. In a synchronous design, this impacts both setup and hold timing closure. In the SleepWalker microcontroller, the depth of the logic paths that are critical for setup constraint is quite large (~70 stages). Therefore, their variability is averaged out [29], [38] and the setup guardband for 3σ robustness with respect to WID variability remains low<sup>2</sup>. However, the logic paths that are critical for hold constraint feature short depths and are thus susceptible to larger variations (σ/μ) , which might result in hold time violations. The hold constraint is defined by [15]

\[ t_{C→Q} + t_{logic} > t_{skew} + t_{hold} \]  

(2)

where \( t_{C→Q} \) is the delay from clock to output of the launch flip-flop, \( t_{logic} \) is the delay of the logic path, \( t_{hold} \) is the hold time requirement of the capture flip-flop, and \( t_{skew} \) is the clock skew between launch and capture flip-flops. The flip-flops in the ULV power domain of SleepWalker have a negative \( t_{hold} \) and the hold time constraint can be rewritten as

\[ t_{skew} < t_{C→Q} + t_{logic} + |t_{hold}|. \]  

(3)

A hold time violation can thus only be caused by a large positive \( t_{skew} \). Even if the nominal skew can be kept under control by the place-and-route tool at the generation of the clock tree (CT), delay variations in the CT result in an unpredictable clock skew that can lead to hold time violations[17]. This can be handled by statistical static timing analysis (SSTA). Due to the non-Gaussian delay distributions at ULV [38], SSTA is highly computationally intensive [15] or require special techniques that are beyond the scope of this paper. We chose instead to design a low-variability CT.

Seok et al. proposed a low-variability CT topology adapted to ULV where a single-stage bufferization at the tree root replaces distributed bufferization [39]. This is possible because RC delays are proportionally lower than gate delays at ULV [30]. However, the clock logic of low-power SoC features, such as clock gating and programmable clock division, can hardly be inserted in such a single-stage bufferization topology without incurring large variability-induced clock skews.

To overcome this limitation, we built a multi-V<sub>th</sub> ULV CT integrating clock gating and clock division logic, as depicted in Fig. 5(a). It is based on the CT topology from [39] with single-stage bufferization, but all CT gates that are inside the clock latency paths are implemented with GP LVT MOSFETs, whereas GP SVT MOSFETs are kept for the CT gates outside the latency path to save leakage power. LVT MOSFETs in the GP process at 0.4 V yield a 2× reduction of both the nominal gate delay (τ<sub>μ</sub>) and its absolute variations (σ). This results in a 2× reduction of the skew variability. To limit the increase of the CT power in active mode to only 6% (due to the higher leakage current of LVT MOSFETs), the drawn gate length L<sub>g</sub> of the LVT MOSFETs is upsize from 60 nm (minimum) to 80 nm.

For clock division, an asynchronous counter is selected for low switching power with an LVT synchronization flip-flop (FF) at the output for low C-to-Q delay insertion and an intermediate LVT buffer for high driving capability. The counter is triggered on clock falling edges to avoid hold hazards at the synchronization FF. Simulations show in Fig. 5(b) that the single-stage bufferization topology and the LVT MOSFETs together reduce skew variations by 3×.

B. ULV SoC Implementation Flow

The full SoC was implemented with Cadence RTL Compiler for physical synthesis and Cadence Encounter for place
and route with a timing-driven CPF-based multimode multi-corner (MMMC) approach, including automatic clock gating insertion. Integrated clock gating cells (IGC) from the foundry libraries were used in the 1-V power domain (AOPs) for low area whereas clock gating blocks where synthesized based on latches to enable the multi-$V_t$ approach required by the proposed clock tree.

To ease the MMMC timing closure, a single nominal PVT corner (TT 0.4 V @25 °C) was considered for the ULV power domain as the AVS compensates most of the delay variations. Worst and best case corners were considered for the 1-V power domain (AOP and memories). The multi-mode was necessary for concurrent power optimization in active and standby modes. Mode transitions (wake-up and sleep) are handled by the sleep controller including start/stop of the AVS system, isolation of output signals from the power-gated ULV power domain, glitch-free synchronization between the crystal clock and the main clock generated on-chip by the CPR ring oscillator. Safe crossing of clock domains is achieved for critical signals with a handshake protocol and double register barriers to limit metastability.

C. ULV Standard-Cell Libraries

To implement the ULV power domain, we generated a dedicated standard-cell library by selecting cells that operate reliably and efficiently at ULV, amongst the cells from the conventional 1 V libraries offered by the foundry. First, to alleviate the noise margin limitation of logic gates at ULV, standard cells with an upsized $L_g$ of 80 nm were selected, which dramatically lowers the functional limit on the supply $V_{lim}$ [17] without the energy penalty incurred by width upsize [21]. The area penalty is only 5% at the scale of the MOSFET (active area) and even lower at the circuit level. The improved noise margins allows the use of standard cells with transistor stacks up to 3, while guaranteeing a high yield with 10 kgates in the ULV power domain. As a result, the generated ULV library uses 82 standard-cell topologies from the original library intended for 1 V operation. Additionally, an upsize of the printed gate length from 60 to 80 nm reduces the MEP energy by ~15% in 65-nm CMOS thanks to subthreshold swing improvement, DIBL reduction and $V_t$ variability mitigation [40]. Second, in the generated library we selected cells with a limited set of driving strengths (up to \times 10 only) to keep power under control at the timing optimization step because low-drive cells feature low leakage power and low switching energy (low

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**Fig. 5.** Proposed SoC CT with corresponding clock latency distributions (Monte Carlo SPICE simulations @0.4 V TT 25 °C).

**Fig. 6.** Die microphotograph of the sub-mm² microcontroller SoC with process, $V_{dd}$, and $I_d$ usage (LP is the thick core oxide process, GP is the thin core oxide process, and $L_g$ values are for drawn gate lengths).
capacitances). Although high-drive cells are useful for speeding up the critical paths, the choice to use only low drive strengths is a way to prevent the tools from prohibitively increasing power consumption to meet timing constraints that are too stringent. Nevertheless, for buffers and inverters all driving strengths are allowed, as these gates need to drive high fan-out nets, especially with the adopted single-stage bufferization CT topology. For density reasons, we did not resize the cells for ULV operation. Instead, we used the original cells from the foundry library as they are highly area optimized. The final library contains 268 selected standard cells that were automatically characterized at the target design point with Synopsys Liberty NCX. Every cell from this library can be used in any of the three $V_t$ options (HVT/SVT/LVT) by CAD layer manipulations.

V. EXPERIMENTAL VALIDATION

The SleepWalker test chip was manufactured in a 7-metal 65-nm LP/GP CMOS process with MIM capacitance option. Fig. 6 shows the die microphotograph with a summary of selected MOSFET type and gate lengths for each partition. The 23 available dies from a TT wafer were successfully tested.

A. CPU and ULV Power Domain Measurements

Fig. 7(a) shows the measured maximum frequency of the ULV power domain including the CPU and instruction cache. It is compared with the 25-MHz/0.4-V design point that was used thanks to the AVS system compensating slow process and low temperature, and to the 25-MHz/0.48-V design point that would be required to ensure the timing closure without the AVS. All 23 dies respect the 25-MHz constraint at the 0.4-V design point. The small guardband between the CPU measurements and the design point with AVS comes from the safety margin taken at design time to ensure high yield with respect to both WID mismatch between the CPR ring oscillator and the actual critical paths and to a potential inaccuracy of BSIM4 MOSFET models in near-$V_t$ regime. This guardband is much smaller than the 80-mV guardband that would be needed to compensate for SS corner at $-40 \degree C$ without the AVS system. The average maximum frequency at 0.5 V is 71 MHz.

As shown in Fig. 7(b), the functional limit $V_{\text{limit}}$ for all 23 dies is below 0.3 V, and the 0.32–0.48-V range for the internal $V_{\text{dd}}$ generated by the AVS system is thus safe. This demonstrates the efficiency of the proposed clock tree to limit hold time violations and of the standard-cell library choices to avoid noise margin degradation. The MEP when operating at the $2\sigma$ worst case frequency (WID variations) and supplied by an external source (AVS disabled) occurs at 23.6 MHz/0.375 V ($f_{\text{MEP}}/V_{\text{MEP}}$) with an $E_{\text{cycle}}$ = 2.2 pJ, when executing an FIR filter using the hardware multiplier [Fig. 7(c)]. The reduced switching activity of NOP reduces $E_{\text{cycle}}$ to 1.85 pJ. Without power gating the GP SVT MOSFETs selected for the ULV domain incurs a leakage power of 33 μW at 0.4 V.

B. AVS System Measurements

The open-loop efficiency of the switched-capacitor DC/DC converter is given in Fig. 8(a). Results are shown for various internal $V_{\text{dd}}$ values ensuring safe operation of the ULV power domain in the SS $-40 \degree C$, TT 25 $\degree C$ and FF 85 $\degree C$ corners, with the length of the variable-length RO swept over the whole range. Each curve exhibits a different range of load current because the difference between $V_{\text{ref}}$ and $V_{\text{out}}$ from (1) is corner-dependent, from 20 mV for the SS $-40 \degree C$ to 180 mV for the FF 85 $\degree C$ corner. However, the power consumption of the ULV domain also depends on the corners. As shown in Fig. 8(a), the converter is able to deliver enough current to the load under all operating conditions, with a safety margin of at least 2x. The converter efficiency varies with the supplied internal $V_{\text{dd}}$ for two reasons, given here.

- The intrinsic efficiency limit of the switched-capacitor converter equals the ratio between $V_{\text{out}}$ of the converter (the internal $V_{\text{dc}}$ of ULV power domain) and $V_{\text{in}}$. The maximum achievable efficiency is thus 96%, 80% and 64% for the following conditions: SS/$-40 \degree C$ at 0.4 8V, TT/25 $\degree C$ at 0.4 V and FF/85 $\degree C$ at 0.32 V, respectively.
- The power overhead of the converter from the variable-length RO, the nonoverlapping clock, the gate drivers and the bottom-plate capacitances is proportional to the switching frequency $f_{\text{sw}}$. At a given $f_{\text{sw}}$ and thus given power overhead, the load current varies with the internal
Fig. 8. Measured DC/DC converter and AVS system results. (a) DC/DC converter efficiency for a 1-V external $V_{dd}$, the arrows show the estimated ULV power domain consumption range for typical and extreme corners. (b) Line @ $I_{out}$ = 155 µA, 25 °C and (c) load @ external $V_{dd}$ = 1 V, 25 °C regulation of internal $V_{dd}$ and main clock frequency, (d) power consumption of the ULV domain (including the DC/DC converter) with and without AVS internal $V_{dd}$ regulation (10 tested dies, at 25 MHz in all conditions).

Fig. 9. Measured transient behavior of the internal $V_{dd}$ at start-up and for a sudden change of the workload (CPU going from performing NOP operations to FIR looping, at 25 °C).

$V_{dd}$. At high internal $V_{dd}$, this power overhead gets associated to lower load currents, which lowers the efficiency. The measured efficiency peaks above 80% for 0.45-V internal $V_{dd}$ and 1-V external $V_{dd}$.

Fig. 8(b) and (c) shows the closed-loop AVS line and load regulation of the main clock frequency and internal $V_{dd}$. The internal $V_{dd}$ is maintained between 398 and 403.4 mV for a load current ranging from 25 to 713 µA or an external $V_{dd}$ ranging from 0.88 to 1.22 V. It corresponds to frequency fluctuations below 3.3% for the microcontroller clock. As the external $V_{dd}$ or the load current changes, the internal $V_{dd}$ varies leading to a frequency deviation of the microcontroller clock. Fig. 8(b) and (c) thus shows how the AVS feedback loop detects a deviation from the target frequency and adapts the length of the converter variable-length RO accordingly. The logarithmic scale on the length increment ensures that only 31 regulation steps can accommodate a wide 30x load current span.

Fig. 8(d) shows the measured $V_{dd}$ guardband reduction achieved by the AVS system on 10 tested dies. An average power saving of 25–30% is achieved, thanks to $V_{dd}$ reductions up to 110 mV, when compared with the 0.48 V worst-case $V_{dd}$ for 25 MHz operation at the –40 °C SS corner.

Fig. 9 shows the transient behavior of the internal $V_{dd}$ at start-up with the start-up steps detailed for illustration purpose. First when the CPU state request signal goes to active, the converter sends charges to the 3.3 nF $C_{out}$. At this stage, the power of the ULV domain is limited to its leakage power. Therefore, the internal $V_{dd}$ rises close to the $V_{dd}$ voltage of the converter (0.5 V). Second, the CPR is started and switching power occurs in the ULV domain, resulting in a small drop of the internal $V_{dd}$. The generated clock is then synchronized with the crystal clock and the operation of the CPU is finally started. The AVS loop starts regulating the CPU frequency at this step. Fig. 9 also shows the AVS loop response to a steep workload in-
crease. In Section III-D, to prove system stability, we assumed a low-power mode with ideal clock gating (no switching at all) as a worst case. This could not be tested in measurement as this mode is not implemented in the test chip. We emulate this mode instead by performing only NOP operations for a 54-μW power consumption. When the workload signal goes high, the CPU runs at full workload by performing FIR looping and consumes 67 μW (with IS power included). When the workload changes, the internal Vdd only falls by 15 mV before going back to 0.4 V. This shows that the results from Section III-D are conservative and that workload fluctuations do not threaten the CPU operation as internal Vdd stays 80 mV above the 0.3-V functional limit.

C. Full SoC Power Measurements

Measurements of the full SoC demonstrate a record power in active mode of 174 μW (average of the 23 tested dies) at 25 MHz, i.e., just below 7 μW/MHz, while keeping the standby power at 1.69 μW. In active mode, the variability (σ/μ) of the switching-dominated power is only 1.2%. In standby mode, the power variability is 7.2% because it is dominated by the leakage power, which is more sensitive to Vdd variations. The contributions of the proposed techniques to the ultra-low active power are summarized in Fig. 10(a). Power breakdowns in active and standby modes are given in Fig. 10(b) and (c), respectively. In active mode, the SoC achieves a nice power balance between the CPU and the memory system. The DC/DC converter only consumes 12% of the total SoC power in active mode while in standby mode its embedded power gating scheme is capable of reducing the leakage power of the ULV power domain by at least 50%. If the SoC is intended to be used in an application with a lower cache hit rate, the active energy of the memories could become prohibitive. In that specific case, an option would be to trade die area for power savings in the memory system by optimizing its architecture as in [41].

D. Comparison With the State of the Art

Table 1 summarizes main performances of SleepWalker compared with the most advanced ultralow-power MSP430 microcontroller from the industry [14] and academic research [15]. The proposed techniques allow SleepWalker to operate at the same speed as the industrial nominal-voltage MSP430...
microcontroller in 0.13-\mu m CMOS, with a 20× improvement in active-mode energy efficiency. Moreover, SleepWalker is 50× faster than the previous 65-nm sub-\textit{V}_\text{t} research MSP430 microcontroller [15], with an energy efficiency that is 3× better. The 25-MHz speed at 0.4 V is enabled by the combination of the GP process for the ULV power domain, the 1-V SRAM operation, the low \textit{T}_{\text{cycle}} guardband thanks to the AVS system, and a timing-driven EDA tool flow with libraries characterized at the target operating points. Finally, the compact design approach in 65-nm CMOS yields significant die area reduction for SleepWalker.

In order to evaluate the benefits brought by this compact design approach from a DfE perspective, we evaluated the embodied energy and carbon footprint of chip manufacturing. Therefore, we used the life-cycle assessment model for CMOS processes from [4], [42], tuned to process technologies relevant for WSN applications. We first considered the 0.13 \mu m CMOS process with embedded NAND Flash as the conventional WSN process in the industry. We further considered a 65 nm LP CMOS process to evaluate the benefits from technology scaling as well as the 65 nm LP/GP CMOS process used for SleepWalker. Despite the slightly more complex process in 65 nm LP/GP, Table I shows that SleepWalker has a 5× lower footprint thanks to the extremely compact die. Notice that the SleepWalker test chip requires an external crystal clock but there is space left on the die that could be used to embed a low-power reference clock generator such as in [43], to avoid the carbon footprint overhead of an external generator.

VI. CONCLUSION

The proposed SleepWalker microcontroller for wireless sensor nodes (WSNs) leverages a 0.4-V ultralow-voltage (ULV) operation at 25 MHz in 65-nm CMOS to achieve sub-mm\textsuperscript{2} die area and a record 7-\mu W/MHz SoC active power compromising neither speed performance, standby power, robustness nor integration level. The dual-\textit{V}_\text{t} multi-\textit{V}_\text{t} partitioning in the LP/GP process mix enables the operation of each system block close to its minimum-energy point under the 25-MHz timing constraint. For low die area and standby power, the dense high-\textit{V}_\text{t} 6 T SRAM bitcell from the foundry with 1-V operation is preferred and its switching power overhead is limited by a synthesized ULV instruction cache. An all-digital on-chip adaptive voltage scaling (AVS) system based on switched-capacitor DC/DC converter efficiently compensates the impact of PVT variations to guarantee the speed of the ULV power domain in all conditions. Robust operation of the full SoC down to 0.3 V is achieved thanks to a dedicated multi-\textit{V}_\text{t} clock tree and a standard-cell library with upsized gate lengths. The carbon footprint for chip manufacturing is reduced by 4–6× when compared with previous industrial and academic microcontrollers, thereby paving the way to a low-carbon deployment of the Internet-of-Things.

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